

A RAPID CHANNEL DETECTION SYSTEM FOR EW RECEIVERS

R.G. Ranson and S.G. Gibbons

Watkins-Johnson Company

Palo Alto, California

ABSTRACT

A new subsystem is described that combines microwave circuits with digital processing to provide ultra fast frequency information in a form suitable for integration into more complex receiver systems.

INTRODUCTION

The rapid, accurate, identification of the input signal frequency is a vital parameter for modern Electronic Warfare (EW) systems. While there are a wide variety of techniques that have been developed to meet diverse system requirements, they generally fall into one of two classes. The first employs broadband techniques to simultaneously cover all frequencies. This maintains a high probability of intercept at the expense of possible overload in dense multiple signal environments. The second class uses narrow band receivers that are swept, or clustered in channels in some way to cover a broad range. This trades off probability of intercept for the ability to filter out certain signals in dense environments.

This paper describes a unique RF/digital subsystem that attempts to combine the merits of these two strategies. It uses a low resolution, ultra fast IFM to provide real time signal frequency information that can be used to dynamically allocate receiver resources. Incorporating this type of subsystem in the RF or IF section of a receiver opens up new possibilities for system architecture by providing useful signal processing capabilities much earlier in the RF chain than was previously possible.

DESCRIPTION OF THE SYSTEM

The channel detection system (channelizer) is essentially a scaled down, low resolution instantaneous frequency measurement (IFM) module, but it also contains other new technology elements that give it its capability. A block diagram of the unit is shown in Figure 1.

An integrated, broadband, limiting amplifier is used to increase the dynamic range and to provide suppression of simultaneous signals. This limiting amplifier uses custom MMICs to provide state-of-the-art limiter performance with low harmonic content and excellent phase response (1). It extends the sensitivity of the IFM to -48 dBm and also contains an RF detector for signal present identification.

The IFM portion uses delay line discriminators integrated in MIC form (Figure 2). Two discriminators are necessary to provide high accuracy and tolerance to simultaneous signals.

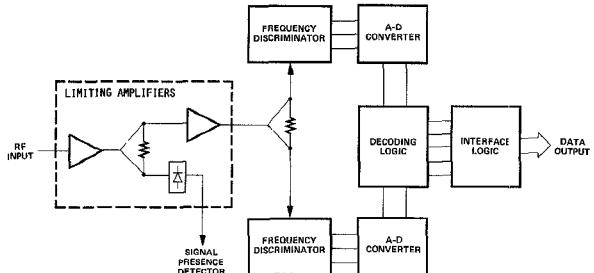


Figure 1. Block Diagram of Channelizer System

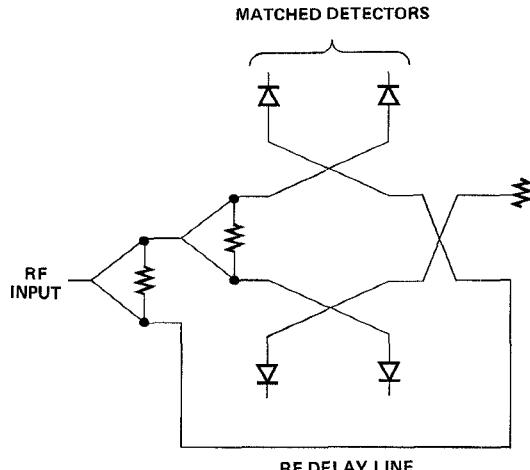


Figure 2. Schematic of Frequency Discriminator

The short delay line discriminator is adjusted for 45 degree quantization in the band. While the longer delay path is adjusted for 90 degree quantization. This partitioning of the phase error budget in favour of the finest resolution discriminator optimizes performance when simultaneous signal are present (2),(3).

The video section uses modern, high speed 686 type comparator ICs in a zero-crossing, flash A-D configuration to digitize the phase information in less than 10 nS. The decoding logic and bus interface is programmed into two 22V10 style Programmable Logic Devices (PLD). These devices provide the equivalent of 500 to 800 gates in one package with propagation delays as low as 15 nS. They are electrically programmable and sufficiently sophisticated that they can be tailored to a wide range of I/O applications (4). The dynamic range compression

of the limiting amplifier, combined with the zero-crossing A-D, makes the digital output essentially independent of input power.

The speed of operation of different parts of the system is summarized in Table 1. Because of the coarse resolution of the discriminators the delay line lengths are very short (<2 nS). The majority of the time is spent in the A-D converter and PLDs. The availability of GaAs comparators and speed enhancements to gate array logic will allow improvements to the channel detection time in the future.

Table 1. Breakdown of System Speed

Limiting Amplifiers	2 nS
Frequency Discriminators	2 nS
Flash A-D Converter	10 nS
PLD	15 nS

OPERATION

The first unit of this type that has been developed covers the 2-6 GHz band, has -48 dBm sensitivity, and identifies signals with ± 30 MHz accuracy to a resolution of 250 MHz, in 30 nS (Figure 3). The photograph in Figure 3 shows the limiting amplifiers and 2 MIC frequency discriminators integrated on one side of the unit. The A-D converter and PLD circuits are on the other side.

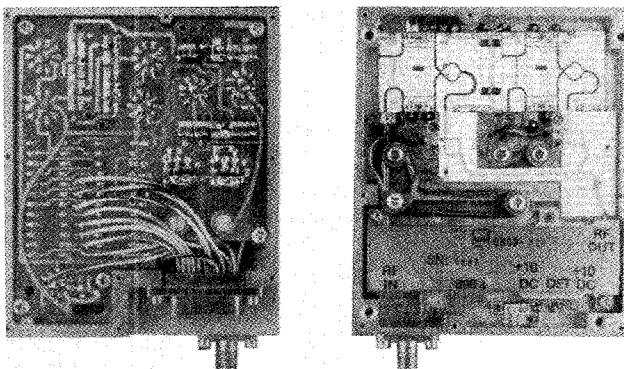


Figure 3. Photograph of the 2-6 GHz Channel Identifier

This prototype is used in the 1st IF of a wideband EW receiver, where it identifies which 250 MHz subband contains the incoming signal and provides digital data to switch an LO generator so that the signal is converted into a narrower 2nd IF band (Figure 4). A suitable delay cable is used in the 1st IF path to allow time for signal identification and LO switching.

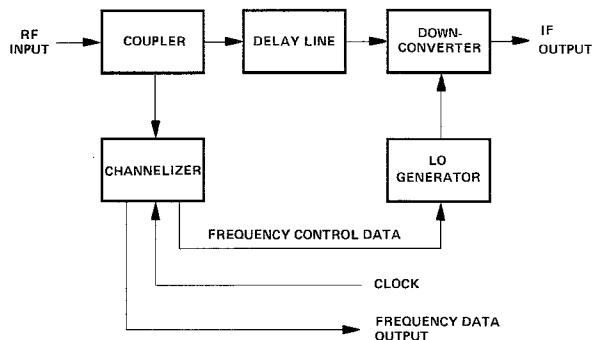


Figure 4. An Example of a Channelizer Application

In its primary mode of operation the channelizer is synchronized by the clock of the system controller. The clock latches data out on a dedicated high speed bus to the LO generator and on a bi-directional binary coded bus back to the controller. There is also a data valid flag generated by the channelizer that indicates the integrity of the data. Time of arrival information is generated either from another part of the system or from the integrated signal presence detector. (Figure 1).

The quality of the limiting amplifier and the method of digitization in the IFM make the channel boundaries virtually independent of any input power level above the -48 dBm threshold. The error in the channel location is shown in Table 2

Table 2. Frequency Accuracy

Channel Number	Channel Edges (MHz)	Measured Edges (MHz)	Error (MHz)
0	2000	1978.1	-22.0
1	2250	2264.9	14.9
2	2500	2513.9	13.9
3	2750	2741.7	-8.4
4	3000	2981.4	-18.1
5	3250	3249.9	0.1
6	3500	3513.6	13.6
7	3750	3729.7	-20.4
8	4000	4002.0	2.0
9	4250	4255.8	5.8
10	4500	4513.6	13.6
11	4750	4740.8	-9.2
12	5000	4993.1	-6.9
13	5250	5252.4	2.4
14	5500	5501.2	1.2
15	5750	5762.7	12.7
	6000	5981.7	-18.4

The speed of the system is illustrated in Figure 5. The oscilloscope photographs show the time between the arrival of a pulse, as measured by the external detector, and when the system can clock the channelizer and receive confirmation of valid output data. In this example the clock pulse was set at 30 nS from the leading edge of the RF pulse and the data valid response was generated after a further 5 nS.

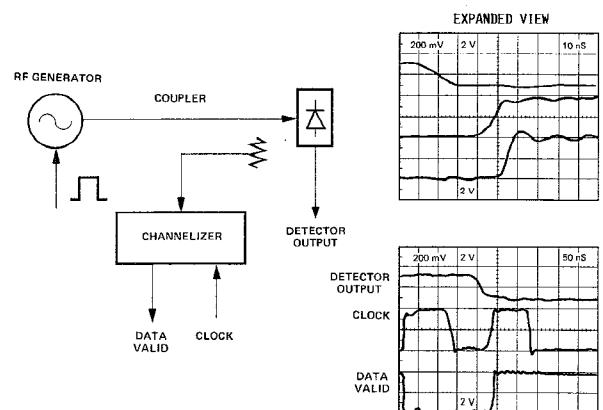


Figure 5. Measurement of Channel Detection Speed

APPLICATIONS

While designed for a specific application the RF channelizer concept has general application in any system requiring real time sorting of frequency information. This flexibility is due to the use of wideband RF circuits and the versatility of the PLD interface.

For example the subsystem in Figure 4 could be applied to a variety of receiver systems depending on the choice of output frequency. Direct conversion to a base band is appropriate for a DRFM application. Similarly, conversion to a UHF band would be suitable for use with a group of channelized or microscan receivers.

There are also potential applications that exploit the output data of the channelizer directly. Figure 6 shows a switched multiplexer that can be used to separate out the identified signal from the IF spectrum (5). This allows separate processing of a piece of the spectrum with the identified signal and the remainder of the spectrum.

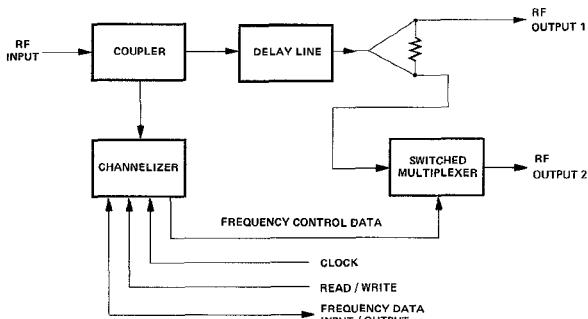


Figure 6. Further Application of Channelizer Concept

The channelizer data interface can also be arranged to receive data and over-ride the identification of the largest signal. This is useful because in many cases the largest signal in the band is one from a friendly, adjacent emitter and both the frequency and time of arrival is known in advance. In this case the EW receiver can be steered to avoid processing irrelevant signals.

CONCLUSION

The channel detection system described in this paper has wide dynamic range, high speed, accuracy and a programmable interface. This is only possible by combining MIC/MMIC circuits with the latest generation of PLDs. It provides new techniques for processing the multitude of signals detected in modern EW receivers. A few applications have been described but it is believed that this type of technique has use in a broad area of adaptive signal processing systems.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the contribution of J.K. Bamford for his efforts in supplying the limiting amplifier for this work and to E.C. Clancy for the mechanical design.

REFERENCES

- (1) E.J. Crescenzi Jr., R.S. Besser, B.A. Tucker, and T.R. Kritzer, "Wideband Limiting Amplifier with Low Second Harmonic Distortion, using GaAs MMIC Limiters", MTT-S International Symposium Digest, pp. 328-331, June 1985.
- (2) P.W. East, "Design Techniques and Performance of digital IFMs", Proc. IEE, Vol. 129, Part F, No. 3, pp. 154-163, June 1982.
- (3) R.G. Ranson, J.G. Galli, and G.L. Hey-Shipton, "Rapid Channel Identifier for the Real Time Sorting of Frequency Data", MSN & CT, pp. 65-73, September 1987.
- (4) Om Agraw et. al., "PLD Programmability Extends its Sway over Complex I/O", Electronic Products Magazine, Vol. 29, No. 24, May 1987.
- (5) C.I. Mobbs, "Matched Four Port Hybrid Filters", MTT-S International Symposium Digest, pp. 149-152, June 1987.